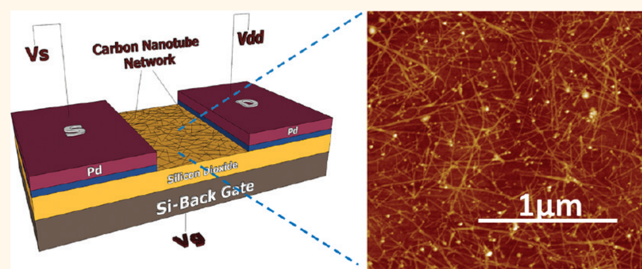
ARTICLE

Wafer-Scale Fabrication and Characterization of Thin-Film Transistors with Polythiophene-Sorted Semiconducting Carbon Nanotube Networks

Luckshitha Suriyasena Liyanage, Hangwoo Lee, Nishant Patil, Steve Park, Subhasish Mitra, Zhenan Bao,* and Hon-Sum Philip Wong*

Center for Integrated Systems, Department of Chemical Engineering and Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States

ABSTRACT



Regio-regular poly(3-dodecylthiophene) wrapped semiconducting SWNTs.

Semiconducting single-walled carbon nanotubes (SWCNTs) have great potential of becoming the channel material for future thin-film transistor technology. However, an effective sorting technique is needed to obtain high-quality semiconducting SWCNTs for optimal device performance. In our previous work, we reported a dispersion technique for semiconducting SWCNTs that relies on regioregular poly(3-dodecylthiophene) (rr-P3DDT) to form hybrid nanostructures. In this study, we demonstrate the scalability of those sorted CNT composite structures to form arrays of TFTs using standard lithographic techniques. The robustness of these CNT nanostructures was tested with Raman spectroscopy and atomic force microscope images. Important trends in device properties were extracted by means of electrical measurements for different CNT concentrations and channel lengths (L_c). A statistical study provided an average mobility of 1 $cm^2/V \cdot s$ and I_{on}/I_{off} as high as 10^6 for short channel lengths ($L_c = 1.5$ μm) with 100% yield. This highlights the effectiveness of this sorting technique and its scalability for large-scale, flexible, and transparent display applications.

KEYWORDS: carbon nanotube network · hybrid nanostructure · stick percolation · thin-film transistor

Single-walled carbon nanotubes (SWCNTs) have gained much attention in thin-film transistor (TFT) technology development due to their high carrier mobility and high current density.[1−5] In addition to superior conductance to a-Si and organic-based materials,[6] thin films of SWNTs are also flexible and transparent, which paves the way for many possibilities for future TFT technology.[4,7] The ease of fabrication with low-cost processing techniques compatible with plastic electronics at room temperature makes CNTs attractive for flexible, transparent display applications.[1,8]

In order to use CNTs as the channel material of future TFT devices, we have to develop effective low-cost solution sorting techniques that can separate semiconducting SWCNTs from the intrinsically metallic and semiconducting mixture of as-produced CNTs. The metallic CNTs are known to short the channel above a percolation threshold.[3,9] They also result in low I_{on}/I_{off} below the percolation threshold. Thus we need pre-enriched semiconducting CNTs to achieve high I_{on}/I_{off} high-performance transistors. In the past, many methods have been investigated to address this issue, including density gradient ultracentrifugation,[10,11] surface sorting,[12] selective growth methods,[13,14] electrical burning,[15] and dielectrophoresis.[16,17] The former two have received much attention lately due to their scalability and solution processing compatibility. We also previously reported a novel, chirality-based sorting technique that relied on regioregular poly-(3-dodecyl thiophene) to aid the dispersion of semiconducting single-walled nanotubes (sc-SWNTs).[18] Our geometric model together with previous experimental observations[19] suggests that rr-P3DDT polymers self-assemble into a supramolecular shell wrapping the sc-SWNTs to form hybrid nanostructures. The high selectivity of sc-SWNT sorting was confirmed by both spectroscopic techniques and electrical measurements. Although the above-mentioned separation methods have been investigated in detail by many groups,

* Address correspondence to zbao@stanford.edu, hspwong@stanford.edu.

Received for review October 3, 2011 and accepted December 9, 2011.

Published online December 09, 2011
10.1021/nn203771u

© 2011 American Chemical Society

our reported sorting technique has yet to be studied beyond device level demonstration for large-scale TFT fabrication and yield.

In this study, we investigate the scalability, robustness, and the device level behavior of the hybrid nanostructures with respect to channel length and concentration. Here we try to answer some key questions that are important for practical applications. We investigate the effect of CNT concentration on device performance. We characterize devices with small channel lengths (L = 1.5 μm) to determine if high I_{on}/I_{off} can be obtained with a satisfactory yield. We evaluate the device properties for different channel lengths. Moreover, we also discuss the effects of standard lithographic techniques on our hybrid nanostructures. Some research groups have used soft lithographic techniques[8] in the past to mitigate the effects of metallic tubes without incorporating any sorting techniques. Others have used ultracentrifugation methods for sorting followed by wafer-scale fabrication of CNT devices for TFTs.[3,20] Those efforts have used pure CNT materials unlike the hybrid nanostructures presented in our work. Since lithographic techniques also incorporate organic polymers as does photoresist (PR) for exposure and development, it was possible for PR to interact with the polymer-wrapped hybrid structures.

In order to address the above potential issues, we have used the aforementioned sorted nanohybrid structures to form TFTs on silicon wafers and extracted device parameters for different concentrations (C) and different channel lengths (L_c). Random CNT networks with controlled solution depositions present reproducible and consistent results with average I_{on}/I_{off} of 3.5×10^5 for small channel lengths of 1.5 μm, which is compatible with the average sorted CNT lengths. Furthermore, our sorting technique does not need any extra process steps to burn away the metallic CNTs after processing due to high purity. With all measured transistors in working condition with $I_{on}/I_{off} > 10$, we conclude our device yield to be 100% after device processing.

RESULTS AND DISCUSSION

In order to explore the compatibility of lithographic techniques on hybrid CNT structures, we fabricated bottom gate TFT devices using the most common lithography patterning techniques. We started with a 4 in. silicon wafer with a thermally grown dry oxide (116 nm) and cleaned with Piranha solution (H_2SO_4/H_2O_2 v/v ratio 9:1) to obtain a hydrophilic surface. The cleaned wafer was then treated with APTMS (aminopropyltrimethoxy silane) to give an amine-functionalized surface. The amine-terminated surfaces are well-known for their ability to interact with CNTs to assist uniform, consistent CNT depositions.[3,21]

After the surface treatment, the wafers were soaked in a diluted P3DDT−SWCNT solution for 5 days. The setup was kept in isolation and not interrupted to obtain uniform tube deposition. Then the wafers were blown dry with N_2 gas and baked in a vacuum oven at 100 °C for 2 h. Device fabrication was followed using standard photolithographic techniques and Ti (1 nm), Pd (60 nm) source and drain metal contacts were formed following a standard lift-off process. Titanium is known for its good nanotube wetting capabilities,[22] while palladium can form ohmic contacts[22,23] with most nanotubes (d > 1.5 nm) to provide minimal contact resistance. CNTs outside the channel region were removed using oxygen plasma etching.

After fabrication, we first determined the effect of lithographic techniques on the sorted CNT network. First, by using atomic force microscopy (AFM) images, we confirmed that sorted CNTs remain on the substrate surface after the lithography steps. During TFT fabrication, the CNTs were held down by the metal contacts after metal deposition; thus it was unclear whether the photoresist removal removed some sorted CNTs. In order to clarify this, we fabricated stripes of CNT channels on silicon wafer with a width of W = 50 μm and channel length of L_c = 4 μm without any metal contacts to provide support. Figure 1 shows the AFM image of such a structure where the CNT network is clearly visible after PR removal and channel isolation. The image illustrates a sharp edge with an average CNT film thickness of 2.3 nm.

In addition, we verified that the same channel area was covered with CNTs using 785 nm Raman mapping technique. For this analysis, we prepared a 5 × 20 μm rectangle shaped CNT film and measured G- and D-mode peak intensities at the positions, as shown in Figure 2a. Figure 2b shows that the dimension of the mapped image is identical to the microscope image. These mapping technique results combined with AFM images provide evidence that some sorted CNTs remain in the channel region after device fabrication; however, it also proves that sorted CNTs are not totally immune to lithographic techniques. The large D-mode peaks in Figure 2c indicate the damage induced by the photoresist removal process on remaining CNTs. The negligible D-mode peak of as-sorted CNTs in the inset shows they are intact before subject to lithography. Thus, the ∼10× reduction in mobility (when compared to our previous study[18] that did not employ lithographic techniques) we experience in our current devices is caused by the partial removal and/or damage induced by this process on sorted CNTs.

Our soaking method results in random CNT networks that transport charge by percolation.[24] Thus we were particularly interested in the trends of ON and OFF currents with respect to device channel lengths (L_c). Therefore, all of our measurements were performed on devices with fixed channel widths (W) of 50 μm for varying channel lengths of L_c = 1.5, 4, 10, and 30 μm. On average, 20 devices were measured for each

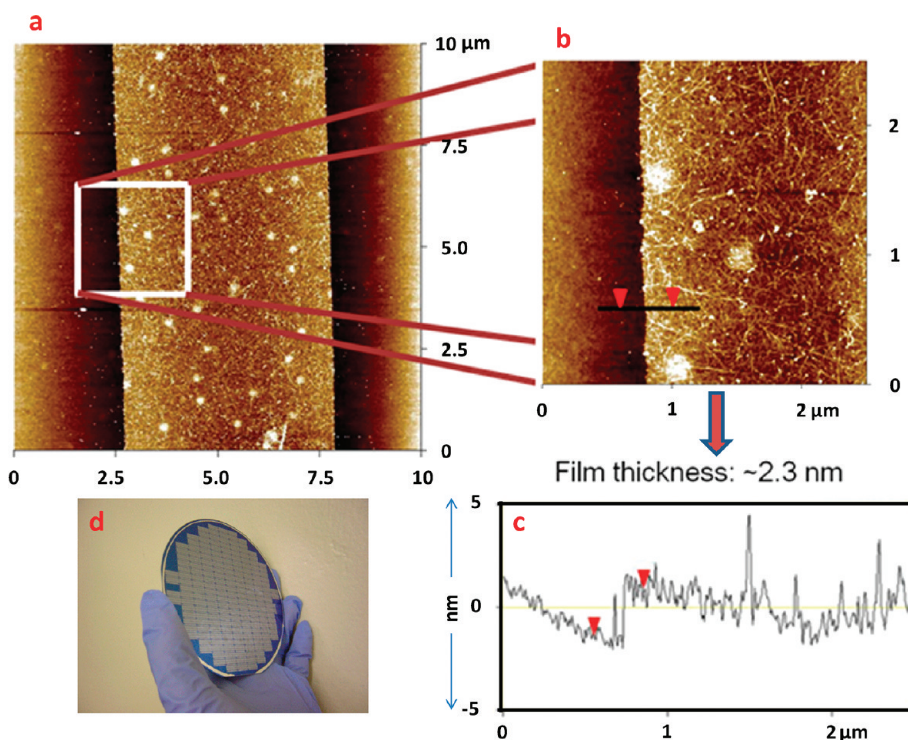


Figure 1. (a) AFM image of a patterned CNT channel region without any source–drain contacts. The measured area of the channel is $10 \times 10\,\mu m^2$. The concentration (C) used for this deposition is 0.1 (as-sorted CNT/toluene ratio is 1:10). (b) Magnified image clearly illustrates a sharp edge which indicates that sorted nanostructures are subject to lithographic techniques. (c) Step profile with an average film thickness of 2.3 nm. (d) Processed silicon wafer with sorted CNTs after Ti, Pd source–drain deposition.

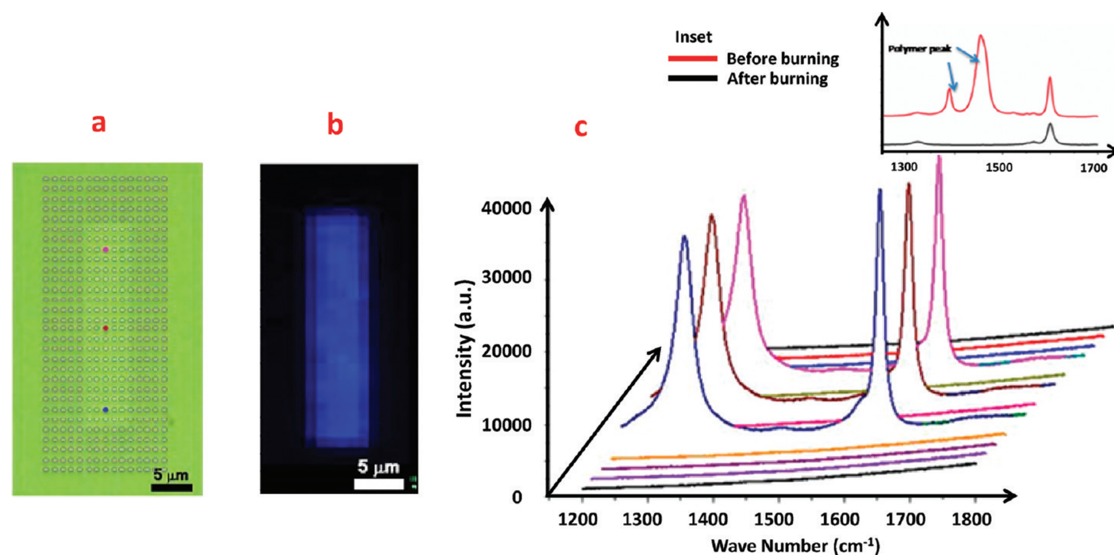


Figure 2. Raman mapping technique that independently verified the effective patterning of hybrid nanostructures. (a) Array of positions in the Raman spectrometer that was programmed to detect a signal. (b) Image prepared after detecting the signal from the scanned array of positions. (c) G-band and the D-band intensities inside the channel region relative to the outside where there are no nanostructures. In creating this map, the Raman scattering spectra used excitation energy of 1.96 eV (633 nm) that resonates with metallic SWNTs and semiconducting SWNTs with nearly a 50/50 ratio. The inset shows the spectra of dispersed supernatant before and after P3DDT burning. The D-band is negligible after polymer burning. However, in the main figure, the D-band is quite large after subject to lithography.

channel length. The CNT network film was patterned to reduce leakage current. Figure 3 shows the electrical measurement results of hybrid CNT-TFTs. Figure 3b,c shows the typical transfer and output characteristics of a device with $W = 50\ \mu m$ and $L_c = 1.5\ \mu m$. For this particular device, the ON current (I_{on}) was 18 μA (0.36 $\mu A/\mu m$) and the OFF current (I_{off}) was 500 pA (10 pA/μm.)

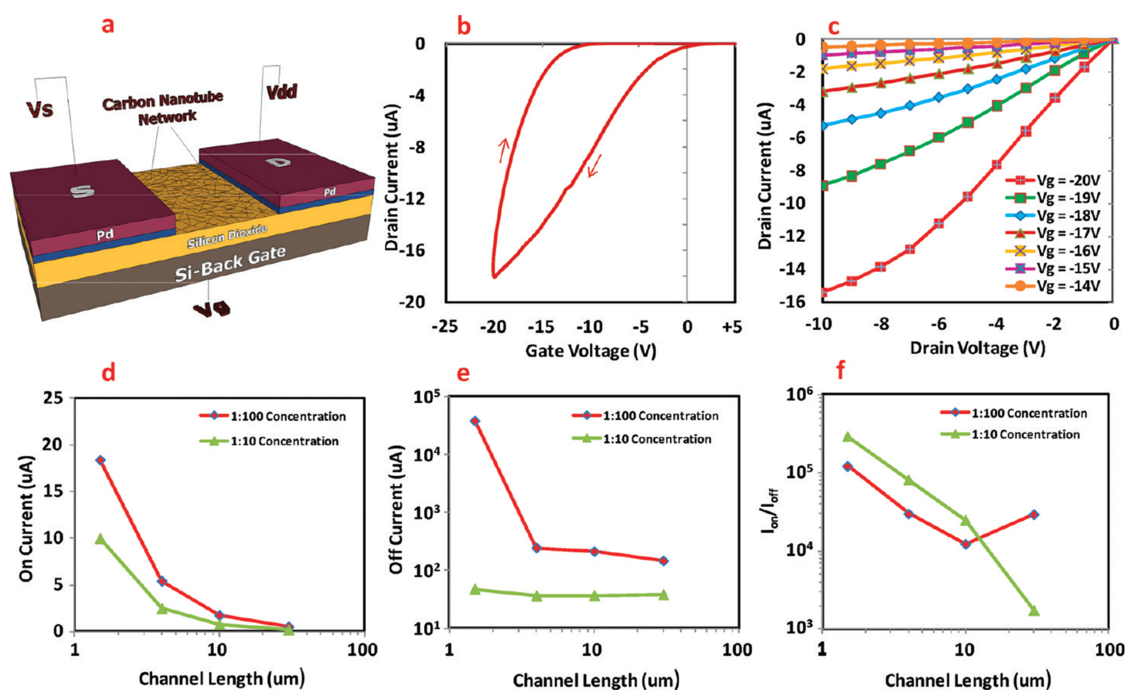


Figure 3. (a) Schematic diagram of the sorted CNT network transistor on top of Si/SiO_2 substrate. All devices have a constant channel width of 50 μm. (b) Typical transfer curve of a CNT-TFT (L_c = 1.5 μm) with mobility of 1 cm^2/V·s and ON–OFF ratio of 3.2 × 10^4. The hysteresis is caused by the surface-bound water molecules under ambient conditions. (c) Output curve for the same device. (d) ON current dependence with respect to channel length for C = 0.1 and 0.01 concentrations. (e) OFF current dependence with respect to channel length for the same concentrations. (f) I_{on}/I_{off} dependence with respect to channel length for the same concentrations.

In order to extract the field-effect mobility, we used the equation for the linear region, $\mu = (L_c/C_{ox}V_{ds}W)g_m$ from the basic MOSFET $I-V$ model. C_{ox}, g_m, and V_{ds} refer to oxide capacitance, transconductance, and the applied source–drain bias, respectively. The continuous CNT network on top of the silicon dioxide during inversion acts as a conducting sheet. Thus gate to channel capacitance is merely the oxide capacitance given by $C_{ox} = \varepsilon_{ox}/t_{ox}$, where ε_{ox} is the silicon dioxide dielectric constant and t_{ox} is the oxide thickness. The transconductance was extracted from the linear region of the transfer curve by curve fitting. We observed a mobility range of 0.2–1.4 cm^2/V·s for our devices with L_c = 1.5 μm. The effective mobility extracted from the linear region for the particular device in Figure 3 was 1 cm^2/V·s, lower than our previous study that did not utilize any lithographic techniques. However, the I_{on}/I_{off} was 3.2 × 10^4, which was impressive for such short channel lengths. Given the thick oxide, we have to apply high gate voltages to obtain similar electric field strengths for comparison with other groups;[3,8] thus our I_{on} is defined at −20 V and I_{off} is defined at +5 V. Our devices also showed large hysteresis under ambient conditions as reported by others. This hysteresis can be attributed to polar molecules, such as water at the interface,[25] that can assist charge transfer between residue silanol groups and the CNTs.[26] Since this is not the focus of our paper, we did not study this effect in detail in this work. Surface passivation with hydrophobic coatings[25] such as PMMA (poly(methylmethacrylate)) has been proven to minimize such hysteresis effects.

In order to understand the dependence of TFT characteristics on channel length and CNT concentration, we prepared two wafers with different CNT concentrations (C) by diluting the as-sorted CNT solution with toluene at 1:10 and 1:100 (volume ratio of as-sorted CNT/toluene). This gives rise to CNT networks of different density. The AFM images of these substrates in Figure 4a,b indicate the difference in CNT density of these samples. Following deposition, devices were fabricated simultaneously on two 4 in. wafers with CNT concentration (C) being the only variable. Figure 3d,e shows the I_{on} and I_{off} we obtained for each channel length by averaging the measurement results of 20 devices equally distributed across the wafer. The I_{on} and I_{off} trends can be explained by the stick percolation theory,[9,24] which assumes CNTs as rigid sticks equally distributed on the substrate. If the CNT network density is above a certain threshold ($\rho_{th} \approx 1/\langle L_s\rangle^2$, L_s = average tube length), the CNTs will provide a continuous conducting path from source to drain. In addition, for a CNT density above ρ_{th}, the number of conduction paths will increase for decreasing L_c values, which in effect increases I_{on} according to a power law of $I_{on} = (1/L_c)^m$. The constant m is called the conductance exponent which usually falls between 1 and 2. At the percolation threshold, this exponent has a value of 1.93,

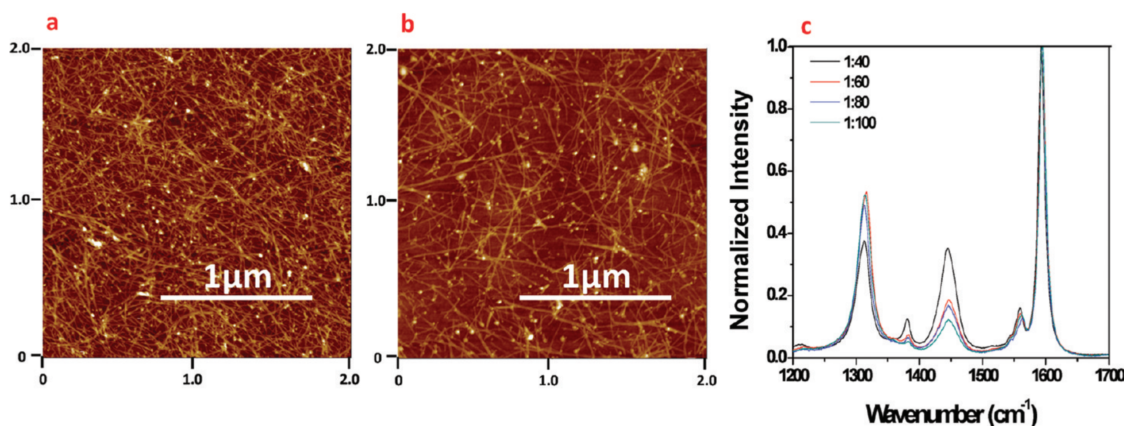


Figure 4. Qualitative comparison between different concentrations. (a) AFM image of high concentration (1:10) CNT network film, (b) AFM image of a low concentration (1:100) CNT network film, (c) Raman spectra of the film, deposited with 1:40, 1:60, 1:80, and 1:100 diluted SWNT solution. The Raman measurement was conducted at excitation of 1.96 eV (633 nm); 1310, 1560, and 1590 cm^{-1} represent D-, G-, and G+ modes by SWNTs; 1380 and 1442 cm^{-1} are due to the C=C symmetric ring stretching of the polymer. The trend is quite clear in the 1442 cm^{-1} peak.

while at very high tube densities, it approaches 1. For our devices, this extracted conducting exponent turned out to be 1.2 for both concentrations, which at first appeared to be a counterintuitive result. According to percolation theory, we expected to get a higher I_{on} and a lower m for devices with high concentration (1:10, $C = 0.1$) than for devices with low concentration (1:100, $C = 0.01$). However, we also need to take into account the presence of the polymer that aggregates around the CNTs in large quantities at higher concentrations. Due to the presence of the polymer, the I_{on} is smaller for a given L_c compared to the CNT network with a similar density. Although rr-P3DDT is also a semiconductor, its charge carrier mobility is much lower than that of the individual CNTs. This causes the overall resistance of the channel to increase. For short channel lengths at high concentration (1:10, $C = 0.1$), we clearly observe a lower I_{on} due to polymer aggregation despite higher CNT density. At this channel length (L_c = 1.5 μm), some tubes probably bridge the metal pads. Thus the polymer seems to have a large effect on contact resistance. As the L_c increases, we have an increasing number of CNT-to-CNT contacts, which are highly resistive due to polymer coverage; therefore, the I_{on} plots for both concentrations decrease with increasing channel lengths.

The same idea can be extended to explain the OFF current trends shown in Figure 3e. The OFF current increases only slightly for both concentrations at long channel lengths due to the high percentage of semiconducting CNT content. However, as L_c becomes smaller and comparable to the average sorted CNT length (L_s = 1 μm), the OFF current shows an increase due to the increasing probability of shorting between source and drain by metallic/semimetallic CNTs. This increase is quite dramatic for the low concentration (1:100, C = 0.01) sample, where the effect of the polymer is low—when the concentration is low, the polymer also has a tendency to detach from the sorted CNTs in solution during soaking. On the contrary, the high concentration (1:10, $C = 0.1$) sample showed only a slight increase due to large impact of the excess polymer. Now that the excess aggregated polymer acts as a resistive semiconducting sheet around the CNTs, they minimize the leakage caused by metallic/semimetallic CNTs thus suppressing the I_{off}.

In order to qualitatively analyze the amount of polymer in different concentrations, we also diluted the sc-SWNT solution with the various volume ratios of 1:40, 1:60, 1:80, and 1:100 (as-sorted SWNT to toluene). After depositing SWNT thin films with the different diluted solutions, Raman measurement was used to characterize the amount of rr-P3DDT present in the sc-SWNT film on the channel. The thiophene polymer mainly showed Raman peaks at 1380 and 1442 cm^{-1} by C=C symmetric ring stretching. After normalization with the G-mode peak intensity of each spectrum, the Raman peak intensities of the polymer were compared with one another. Figure 4c shows that the more diluted the SWNT solution, the less Raman intensities of the polymer.

Since we have almost perfect removal of metallic tubes from this technique, our devices tend to provide larger I_{on}/I_{off} values for smaller channel lengths. This result differs from the usual trend demonstrated by other sorting methods where I_{on}/I_{off} decreases for smaller L_c due to the existence of metallic CNTs.

The sorted, hybrid nanostructures shows this trend because

1. I_{off} is almost constant at OFF state because of high purity of sc-SWNT and the presence of the polymer.
2. I_{on} increases for smaller channel lengths due to the increasing number of conducting paths. Since I_{off} is constant, I_{on}/I_{off} follows the same trend as I_{on}.

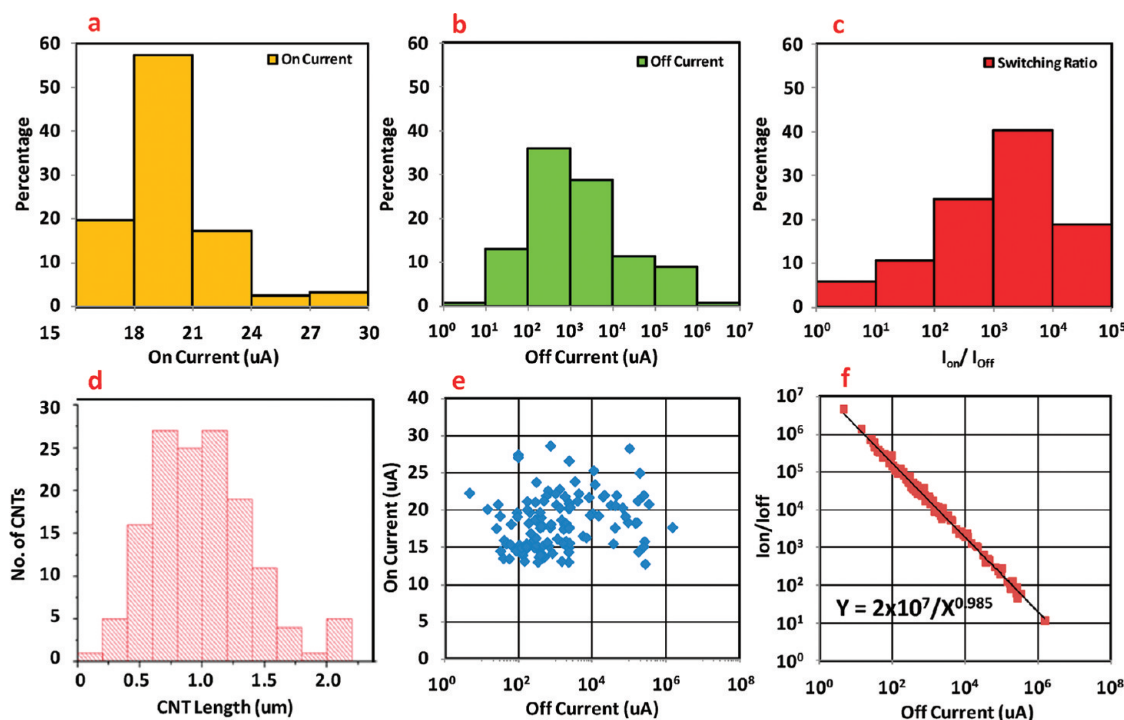


Figure 5. Statistical study of 122 devices with small channel lengths of $L_c = 1.5$ μm, which is comparable to average nanotube lengths. (a) Histogram for ON currents. (b) Histogram for OFF currents. (c) Histogram for I_{on}/I_{off} ratios. (d) Length distribution of 150 sorted SWNTs according to SEM image scans. The samples are prepared by spin-coating at 3000 rpm for 3 min, and annealed for 90 s at 90 °C. The average length of the sorted SWNTs is 0.9997 $\pm$ 0.3999 μm. (e) Distribution of ON current and OFF currents. (f) I_{on}/I_{off} dependence on OFF current. The correlation is quite obvious in this case.

This further demonstrates that sorted CNTs are preferred to obtain high I_{on}/I_{off} at smaller channel lengths. We further explored the effectiveness of our new sorting technique by carrying out extensive device measurements for channel lengths of 1.5 μm. In order to minimize the effect of the polymer, we used devices with $C = 0.1$ (as-sorted CNT/toluene 1:10) that closely resemble the conventional CNT network trends. Figure 5a-c shows the histograms of I_{on}, I_{off}, and I_{on}/I_{off} of 122 devices, respectively. Figure 5d shows a distribution of sorted CNT lengths measured by atomic force microscopy. The average CNT length is 0.997 μm, and some CNTs are even close to 2 μm. At $L_c = 1.5$ μm, we can expect some of those CNTs to bridge source and drain depending on tube alignment. Thus the I_{on}/I_{off} will be determined to be significantly influenced by the effectiveness of the sorting process in such short channel lengths.

According to the histograms in Figure 5, it is apparent that I_{on} has a smaller range and a much tighter distribution when compared to the I_{off} distribution. More than 75% of the devices have ON currents between 15 μA (0.3 μA/μm) and 25 μA (0.5 μA/μm). This tight distribution is due to the uniform deposition of CNTs in the channel. As long as the network is dense and all tubes conduct in the ON state, the impact of the CNT type (metallic or semiconducting) is minimal. The OFF currents, on the other hand, have a wider distribution that surpasses several orders of magnitude because the OFF state is more sensitive to the tube type especially in the channel length at $L_c = 1.5$ μm.

For example, in this regime, if the channel happens to have purely semiconducting CNTs, then the device has a high probability to have smaller OFF state currents. If by chance the channel consists of a few metallic or semimetallic CNTs, the I_{off} can be extremely high. According to the I_{off} distribution, 0.82% of the devices have a chance of having an OFF current greater than 1 μA (0.02 μA/μm). Figure 5e shows I_{on} *versus* I_{off}, where data points are distributed equally on all sides. The calculated correlation coefficient is 0.2, which suggests the I_{on} and I_{off} are almost independent from each other. Figure 5f plots I_{on}/I_{off} *versus* I_{off}, where we see a strong correlation between the two parameters. The calculated correlation coefficient is -0.997, which suggests a linear decrease in I_{on}/I_{off} with an increase in I_{off}. The power series fit to the data points also provides a similar result of $I_{on}/I_{off} = 2 \times 10^7/I_{off}$ (pA), which again suggests that I_{on} behaves as a constant value around 20 μA (0.4 μA/μm) when compared to I_{off}, which is the critical factor that determines the I_{on}/I_{off}. This further emphasizes the importance of developing sorting techniques that can give rise to tight chirality distributions that consist of s-CNTs, especially if we expect to obtain low OFF state currents and high switching ratios for small channel lengths.

In summary, we have fabricated bottom gate thin-film transistors on silicon substrates with chemically

sorted carbon nanotube networks. Electrical measurements, AFM, and Raman spectroscopy verify that lithographic techniques could be utilized for polythiophene-sorted CNT−TFT fabrication, although it might partially degrade the device performance. Concentration and channel variations are shown to provide consistent and predictable results. The I_{on}, I_{off}, and I_{on}/I_{off} trends with respect to CNT concentration and channel length were extracted. Trends observed were explained by means of stick percolation theory. The inverse trends in OFF current and I_{on}/I_{off} ratios with respect to channel lengths arise due to the highly effective sorting mechanism and also due to the presence of rr-P3DDT polymer at different concentrations. In addition, we also demonstrated that, with controlled deposition, well-sorted (high-purity) CNTs can provide moderate mobility and high I_{on}/I_{off} ratio transistors with 100% yield for small channel lengths. With further tuning of sorting and proper processing techniques, such devices can pave the way for cheap, high-resolution, low-power, flexible display applications. This study highlights the importance of advanced study of dispersion-based CNT sorting techniques and provides insight into how such methods can be utilized in the large-scale display electronics market in the future.

EXPERIMENTAL METHODS

Sorted CNT Solution Preparation. Both the polymer and the nanotubes we used in this study are commercially available. The regioregular poly(3-alkylthiophenes) (rr-P3ATs) were purchased from Sigma Aldrich, Inc., and purified HiPCO SWCNT was purchased from Unidym Inc. First we measured 5 mg of rr-P3DDT, mixed it with 10 mL of toluene, and kept it in an oven (70 °C) for complete dissolution. HiPCO SWCNT (5 mg) was then mixed to the above prepared solution, and the complete volume was brought up to 25 mL by addition of toluene, so that the final concentration was 0.2 mg/mL for each material. This suspension was kept in a temperature-controlled cooling bath and sonicated (Cole Parmer ultrasonic processor 750 W) for 30 min at an amplitude level of 70%. The solution was subsequently centrifuged (Sorvall RC5C-plus) for 90 min at 17 000 rev/min, and the supernatant was collected for device fabrication. Additional toluene was added to obtain different concentrations (1:10 and 1:100) relative to the as-dispersed solution for device fabrication.

Raman Measurements. The resonant Raman scattering measurements (RRS, Model: LabRam Aramis from Horiba Jobin Yvon) was carried out at 2.33 eV (532 nm), 1.96 eV (633 nm), and 1.58 eV (785 nm) excitation at 100× magnification, 1 μm spot size, and 1200 grating. Excitation power was 3 mW for the 2.33 eV line, 5 mW for the 1.96 eV line, and 25mW for the 1.58 eV line. The peak positions were calibrated with the Si line at 521 cm^{-1}.

Substrate Preparation (Piranha and APTMS Treatment). In order to promote the adhesion of SWNTs onto the wafers, the SiO_2 surfaces were coated with a monolayer of 3-aminopropyltrimethoxysilane (APTMS). Here, the exposed amine groups of the APTMS monolayer have previously been demonstrated to enhance the binding of SWNTs.[27−29] Prior to APTMS treatment, the substrates were immersed in piranha solution (3:1 ratio of sulfuric acid/hydrogen peroxide) for 25−30 min, rinsed with running deionized water for 10 min, blow-dried with N_2 gas, and placed in a vacuum oven at 100 °C for 30 min. Thereafter, the substrates were placed into a glovebox and subsequently into a solution of 0.4 vol % APTMS (Gelest Inc.) in anhydrous toluene for 45 min. Next, the substrates were rinsed several times with anhydrous toluene and were taken out of the glovebox. Finally, the substrates were immersed in toluene, sonicated for 10 min to remove any multilayers, blow-dried with N_2 gas, and placed in vacuum oven for 30 min at 100 °C.

CNT Deposition. The sorted CNT solution was diluted with toluene (CNT to toluene volume ratios of 1:10 and 1:100) to obtain different CNT/polymer concentrations. The solution was sonicated while being mixed to prevent aggregation of nanotubes during the dilution process. Then the APTMS-treated substrates were immersed into diluted nanotube solution, sealed, and left undisturbed for a week. The samples were then blow-dried with N_2 gas and vacuum-baked for another 30 min at 100 °C before device fabrication.

Device Fabrication. After CNT deposition, a layer of LOL-2000 (Microchem) was spun on the baked silicon wafer (3000 rpm, 60 s). Photoresist exhibits poor adhesion to silicon dioxide and needs an adhesion promoter (*e.g.*, HMDS, hexamethyldisilazane). With LOL-2000, no adhesion promoter is needed. After coating the wafer with LOL-2000, the wafer is then baked at ∼250 °C for 30 min. Next, g-line photoresist (SPR 3612, Microchem) is spun on the wafer (5500 rpm, 30 s). After exposure (55 mJ/cm^2), the wafers were developed in Microposit MF-26A (Microchem) developer for a total develop time of 50 s. Afterward, a bilayer of Ti (10 nm) and Pd (50 nm) was deposited and source−drain electrodes were formed using the lift-off process. Another lithography step was carried out, and CNTs outside the electrode regions were removed using a low-intensity O_2 plasma (30 W, 150 mTorr, 20 sccm O_2, 90 s) using photoresist as a mask. For this step, no LOL-2000 was used (hence, an adhesion promoter (HMDS) was applied in the gas phase to improve the adhesion of the photoresist).

Acknowledgment. The authors thank F. Yap, S. Morishita, A. Lin, H. Wang, and P. Weerasekara for experimental support and enlightening discussions. Work was performed in part at the Stanford Nanofabrication Facility, a member of the NSF-supported National Nanotechnology Infrastructure Network. The work was partly funded by The Center on Functional Engineered Nano Architectonics (FENA), the Samsung Advanced Institute of Technologies, National Science Foundation (ECCS 0901414), and National Science Foundation (Award Number: 1059020).

Supporting Information Available: Polymer wrapping configuration, fabrication process, unsorted CNT characteristics, and CNT diameter information. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Gruner, G. Carbon Nanotube Films for Transparent and Plastic Electronics. *J. Mater. Chem.* **2006**, *16*, 3533–3539.
2. Bo, X. Z.; Lee, C. Y.; Strano, M. S.; Goldfinger, M; Nuckolls, C.; Blanchet, G. B. Carbon Nanotubes-Semiconductor Networks for Organic Electronics: The Pickup Stick Transistor. *Appl. Phys. Lett.* **2005**, *86*, 182102-1–182102-3.
3. Wang, C.; Zhang, J. L.; Ryu, K. M.; Badmaev, A.; De Arco, L. G.; Zhou, C. Wafer-Scale Fabrication of Separated Carbon Nanotube Thin-Film Transistors for Display Applications. *Nano Lett.* **2009**, *9*, 4285–4291.
4. Cao, Q.; Hur, S. H.; Zhu, Z. T.; Sun, Y. G.; Wang, C. J.; Meitl, M. A.; Shim, M.; Rogers, J. A. Highly Bendable, Transparent Thin-Film Transistors That Use Carbon-Nanotube-Based Conductors and Semiconductors with Elastomeric Dielectrics. *Adv. Mater.* **2006**, *18*, 304–309.
5. Snow, E. S.; Novak, J. P.; Campbell, P. M.; Park, D. Random Networks of Carbon Nanotubes as an Electronic Material. *Appl. Phys. Lett.* **2003**, *82*, 2145–2147.

6. Kagan, C. R.; Andry, P. *Thin-Film Transistors*; Marcel Dekker: New York, 2003.
7. Kim, S.; Ju, S.; Back, J. H.; Xuan, Y.; Ye, P. D.; Shim, M.; Janes, D. B.; Mohammadi, S. Fully Transparent Thin-Film Transistors Based on Aligned Carbon Nanotube Arrays and Indium Tin Oxide Electrodes. *Adv. Mater.* **2009**, *21*, 564–568.
8. Cao, Q.; Kim, H. S.; Pimparkar, N.; Kulkarni, J. P.; Wang, C. J.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. Medium-Scale Carbon Nanotube Thin-Film Integrated Circuits on Flexible Plastic Substrates. *Nature* **2008**, *454*, 495–500.
9. Kumar, S.; Murthy, J. Y.; Alam, M. A. Percolating Conduction in Finite Nanotube Networks. *Phys. Rev. Lett.* **2005**, *95*, 066802-1–066802-4.
10. Arnold, M. S.; Green, A. A.; Hulvat, J. F.; Stupp, S. I.; Hersam, M. C. Sorting Carbon Nanotubes by Electronic Structure Using Density Differentiation. *Nat. Nanotechnol.* **2006**, *1*, 60–65.
11. Arnold, M. S.; Stupp, S. I.; Hersam, M. C. Enrichment of Single-Walled Carbon Nanotubes by Diameter in Density Gradients. *Nano Lett.* **2005**, *5*, 713–718.
12. LeMiex, M. C.; Roberts, M.; Barman, S.; Jin, Y. W.; Kim, J. M.; Bao, Z. N. Self-Sorted, Aligned Nanotube Networks for Thin-Film Transistors. *Science* **2008**, *321*, 101–104.
13. Ding, L.; Tselev, A.; Wang, J. Y.; Yuan, D. N.; Chu, H. B.; McNicholas, T. P.; Li, Y.; Liu, J. Selective Growth of Well-Aligned Semiconducting Single-Walled Carbon Nanotubes. *Nano Lett.* **2009**, *9*, 800–805.
14. Li, Y. M.; Mann, D.; Ronaldi, M.; Kim, W.; Ural, A.; Hung, S.; Javey, A.; Cao, J.; Wang, D. W.; Yenilmez, E.; *et al.* Preferential Growth of Semiconducting Single-Walled Carbon Nanotubes by a Plasma Enhanced CVD Method. *Nano Lett.* **2004**, *4*, 317–321.
15. Patil, N.; Lin, A.; Zhang, J.; Wei, H.; Anderson, K.; Wong, H.-S. P.; Mitra, S. VMR: VLSI-Compatible Metallic Carbon Nanotube Removal for Imperfection-Immune Cascaded Multi-Stage Digital Logic Circuits Using Carbon Canotube FETs. *Proc. IEDM* **2009**, 573–576.
16. Krupke, R.; Hennrich, F.; Lohneysen, H. V.; Kappes, M. M. Separation of Metallic from Semiconducting Single-Walled Carbon Nanotubes. *Science* **2003**, *301*, 344–347.
17. Krupke, R.; Hennrich, F.; Weber, H. B.; Kappes, M. M.; Lohneysen, H. V. Simultaneous Deposition of Metallic Bundles of Single-Walled Carbon Nanotubes Using ac-Dielectrophoresis. *Nano Lett.* **2003**, *3*, 1019–1023.
18. Lee, H.; Yoon, Y.; Park, S.; Oh, J. H.; Hong, H. S.; Liyanage, L. S.; Wang, H.; Morishita, S.; Patil, N.; Park, Y.; *et al.* Selective Dispersion of High Purity Semiconducting Single-Walled Carbon Nanotubes with Regioregular Poly(3-alkylthiophene)s. *Nat. Commun.* **2011**, 1545.
19. Giulianini, M.; Waclawik, E. R.; Bell, J. M.; Crescenzi, M.; Castrucci, P.; Scarselli, M.; Motta, N. Regioregular Poly-(3-hexyl-thiophene) Helical Self-Organization on Carbon Nanotubes. *Appl. Phys. Lett.* **2009**, *95*, 013304-1–013304-3.
20. Engel, M.; Small, J. P.; Steiner, M.; Freitag, M.; Green, A. A.; Hersam, M. C.; Avouris, P. Thin-Film Nanotube Transistors Based on Self-Assembled, Aligned, Semiconducting Carbon Nanotube Arrays. *ACS Nano* **2008**, *2*, 2445–2452.
21. LeMieux, M. C.; Roberts, M.; Barman, S.; Jin, Y. W.; Kim, J. M.; Bao, Z. Self-Sorted, Aligned Nanotube Networks for Thin-Film Transistors. *Science* **2008**, *321*, 101–104.
22. Zhang, Y.; Franklin, N. W.; Chen, R. J.; Dai, H. Metal Coating on Suspended Carbon Nanotubes and Its Implication to Metal–Tube Interaction. *Chem. Phys. Lett.* **2000**, *331*, 35–41.
23. Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Wang, D. W.; Gordon, R. G.; Lundstrom, M.; Dai, H. Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-*K* Gate Dielectrics. *Nano Lett.* **2004**, *4*, 447–450.
24. Kocabas, C.; Pimparkar, N.; Yesilyurt, O.; Kang, S. J.; Alam, M.; Rogers, J. A. Experimental and Theoretical Studies of Transport through Large Scale, Partially Aligned Arrays of Single-Walled Carbon Nanotubes in Thin Film Type Transistors. *Nano Lett.* **2007**, *7*, 1195–1202.
25. Kim, W.; Javey, A.; Vermesh, O.; Wang, O.; Li, Y. M.; Dai, H. Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors. *Nano Lett.* **2003**, *3*, 193–198.
26. Lee, J. S.; Ryu, S.; Yoo, K.; Choi, I. S.; Yun, W. S.; Kim, J. Origin of Gate Hysteresis in Carbon Nanotube Field-Effect Transistors. *J. Phys. Chem. C* **2007**, *111*, 12504–12507.
27. Liu, J.; Casavant, M. J.; Cox, M.; Walters, D. A.; Boul, P.; Lu, W.; Rimberg, A. J.; Smith, K. A.; Colbert, D. T.; Smalley, R. E. Controlled Deposition of Individual Single-Walled Carbon Nanotubes on Chemically Functionalized Templates. *Chem. Phys. Lett.* **1999**, *303*, 125–129.
28. Park, S.; Wang, W. M.; Bao, Z. Parallel Fabrication of Electrode Arrays on Single-Walled Carbon Nanotubes Using Dip-Pen-Nanolithography-Patterned Etch Masks. *Langmuir* **2010**, *26*, 6853–6859.
29. Wang, W. M.; LeMieux, M. C.; Selvarasah, S.; Dokmeci, M. R.; Bao, Z. Dip-Pen Nanolithography of Electrical Contacts to Single-Walled Carbon Nanotubes. *ACS Nano* **2009**, *3*, 3543–3551.